What is claimed is:

1. A row decoder of a CMOS image sensor, the row decoder addressing to a plurality of pixels arranged in rows and columns in a CMOS image sensor, the row decoder including a plurality of unit arrays, wherein a unit array comprises:

a first NAND gate for generating a reset gate signal in response to an address signal and a reset signal;

a second NAND gate for generating a selection gate signal in response to the address signal and a selection signal;

a first latch for resetting an output thereof in response to an address latch signal and latching the address signal as the output in response to the address latch signal and the address signal;

a third NAND gate for receiving the address signal and a transmitted signal;

a fourth NAND gate for receiving the output of the latch and a shutter transmitted signal; and

an OR gate for receiving the outputs of the third and fourth NAND gates and generating a transmitted gate signal.

2. The row decoder of claim 1, wherein the latch is an S-R latch.

3. The row decoder of claim 1, wherein the latch latches the address signal during a black interval of a horizontal synchronization signal.

4. The row decoder of Claim 1, the unit array further comprising:

a second latch for resetting an output thereof in response to the address latch signal and latching the address signal as the output in response to a second address latch signal and the address signal; and

a fifth NAND gate for receiving the output of the second latch and a second shutter transmitted signal;

wherein the OR gate is for receiving the outputs of the third through fifth NAND gates and generating the transmitted gate signal.

5. The row decoder of claim 4, wherein the first and second latches are S-R latches.

6. The row decoder of claim 4, wherein the first and second latches latch the address signal during a black interval of a horizontal synchronization signal.

7. A method of image sensing comprising:

imaging a plurality of pixels arranged in rows and columns of a CMOS image sensor;

decoding a row address for at least one of the plurality of pixels by generating a corresponding address signal;

generating a reset gate signal in response to the address signal and a reset signal;

generating a selection gate signal in response to the address signal and a

selection signal;

resetting a latch output signal in response to an address latch signal;

latching the address signal as the latch output signal in response to the address latch signal and the address signal; and

generating a transmitted gate signal in response to the address signal, a transmitted signal, the latched output signal, and a shutter transmitted signal.

8. A method as defined in Claim 7 wherein the latching uses an S-R latch.

9. A method as defined in Claim 7 wherein latching the address signal occurs during a black interval of a horizontal synchronization signal.

10. A method as defined in Claim 7, further comprising:

resetting a second latched output signal in response to the address latch signal;

latching the address signal as the second latch output signal in response to a second address latch signal and the address signal;

receiving the second latched output signal and a second shutter transmitted signal; and

generating the transmitted gate signal in response to the address signal, the transmitted signal, the latched output signal, the shutter transmitted signal, the second latched output signal, and the second shutter transmitted signal.

11. A method as defined in Claim 10 wherein latching the address signal as

the second latch output signal uses an S-R latch.

12. A method as defined in Claim 10 wherein latching the address signal as the second latch output signal occurs during a black interval of a horizontal synchronization signal.

13. A CMOS image sensor comprising:

a plurality of pixels arranged in rows and columns;

a row decoder in signal communication with the plurality of pixels for generating an address signal; and

a plurality of unit arrays in signal communication with the row decoder, each unit array comprising:

a first NAND gate for generating a reset gate signal in response to the address signal and a reset signal;

a second NAND gate for generating a selection gate signal in response to the address signal and a selection signal;

a first latch for resetting an output thereof in response to an address latch signal and latching the address signal as the output in response to the address latch signal and the address signal;

a third NAND gate for receiving the address signal and a transmitted signal;

a fourth NAND gate for receiving the output of the latch and a shutter transmitted signal; and

an OR gate for receiving the outputs of the third and fourth NAND gates and generating a transmitted gate signal.

14. A unit array as defined in Claim 13 wherein the latch is an S-R latch.

15. A unit array as defined in Claim 13 wherein the latch latches the address signal during a black interval of a horizontal synchronization signal.

16. A unit array as defined in Claim 13, further comprising:

a second latch for resetting an output thereof in response to the address latch signal and latching the address signal as the output in response to a second address latch signal and the address signal; and

a fifth NAND gate for receiving the output of the second latch and a second shutter transmitted signal;

wherein the OR gate is for receiving the outputs of the third through fifth NAND gates and generating the transmitted gate signal responsive thereto.

17. A unit array as defined in Claim 16 wherein the first and second latches are S-R latches.

18. A unit array as defined in Claim 16 wherein the first and second latches latch the address signal during a black interval of a horizontal synchronization signal.

19. A row decoder of a CMOS image sensor for addressing a plurality of pixels arranged in rows and columns, the row decoder including a plurality of unit arrays, each unit array comprising:

gate reset means for generating a reset gate signal in response to an address signal and a reset signal;

gate selection means for generating a selection gate signal in response to the address signal and a selection signal;

first latch reset means for resetting a latch output signal in response to an address latch signal;

first latch set means for latching the address signal as the latch output signal in response to the address latch signal and the address signal; and

gate transmission means for generating a transmitted gate signal in response to the address signal, a transmitted signal, the latched output signal, and a shutter transmitted signal.

20. A unit array as defined in Claim 19 wherein the latch set means comprises an S-R latch.

21. A unit array as defined in Claim 19 wherein the latch set means latches the address signal during a black interval of a horizontal synchronization signal.

22. A unit array as defined in Claim 19, further comprising:

second latch reset means for resetting a second latched output signal in

response to the address latch signal;

second latch set means for latching the address signal as the second latched output signal in response to a second address latch signal and the address signal; and

gate transmission means for generating the transmitted gate signal in response to the address signal, the transmitted signal, the latched output signal, the shutter transmitted signal, the second latched output signal, and a second shutter transmitted signal.

23. A unit array as defined in Claim 22 wherein the second latch set means comprises an S-R latch.

24. A unit array as defined in Claim 22 wherein the second latch set means latches the address signal during a black interval of a horizontal synchronization signal.